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POwer SEmiconductors Italian COrporation

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HIGH CURRENT PHASE CONTROL THYRISTOR INSULATED MODULE

AZT400HVI

- Full hermetic packaging
- Base plate insulation uisng AIN substrate
- Industrial compatible packaging
- Contract screws available on request

Repetitive voltage up to	**4500 V**
Mean on-state current	**400 A**
Surge current	**11 kA**

TARGET SPECIFICATION

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Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
$V_{RRM / DRM}$	Repetitive peak reverse/off-state voltage		125	4500	V
V_{RSM}	Non-repetitive peak reverse voltage		125	4600	V
$I_{RRM / DRM}$	Repetitive peak reverse/off-state current		125	100	mA
CONDUCTING					
$I_{T (AV)}$	Mean on-state current	180° sin, 50Hz, Tc=85°C		400	A
$I_{T (AV)}$	Mean on-state current	180° sin. 50Hz, Tc=55°C		590	A
I_{TSM}	Surge on-state current	sine wave, 10 ms	125	11	kA
$I^2 t$	$I^2 t$	without reverse voltage		605 x1E3	A^2s
V_T	On-state voltage	On-state current = 1800 A	25	2,66	V
$V_{T(TO)}$	Threshold voltage		125	1,20	V
r_T	On-state slope resistance		125	0,700	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% VDRM up to 1050 A, gate 10V 5 ohm	125	400	A/µs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	125	1000	V/µs
td	Gate controlled delay time, typical	VD = 100V, gate source 25 V, 10 ohm , tr = 0.5 µs	25	3	µs
tq	Circuit commutated turn-off time, typical	dV/dt = 20 V/µs linear up to 75% VDRM		350	µs
Q_{rr}	Reverse recovery charge	di/dt = -20 A/µs, I = 700 A	125		µC
I_{rr}	Peak reverse recovery current	VR = 50 V			A
I_H	Holding current, typical	VD = 5V, gate open circuit	25		mA
I_L	Latching current, typical	VD = 5 V, tp = 30 µs	25		mA
GATE					
V_{GT}	Gate trigger voltage	VD = 5 V	25	3,5	V
I_{GT}	Gate trigger current	VD = 5 V	25	400	mA
V_{GD}	Non-trigger gate voltage, min.	VD = VDRM	125	0,25	V
V_{FGM}	Peak gate voltage (forward)			30	V
I_{FGM}	Peak gate current			10	A
V_{RGM}	Peak gate voltage (reverse)			5	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs		150	W
P_G	Average gate power dissipation			2	W
MOUNTING					
$R_{th(j-c)}$	Thermal impedance, DC	Junction to case		51	°C/kW
$R_{th(c-h)}$	Thermal impedance	Case to heatsink		20	°C/kW
T_j	Operating junction temperature			-30 / 125	°C
V_{ins}	RMS insulation voltage	50Hz, circuit to base,all terminal shorted	25	6000	V
T	Mounting tourque	Case to heatsink		4 to 6	Nm
	Mass			2800	g

ORDERING INFORMATION : AZT400HVI S 45

standard specification — VDRM&VRRM/100

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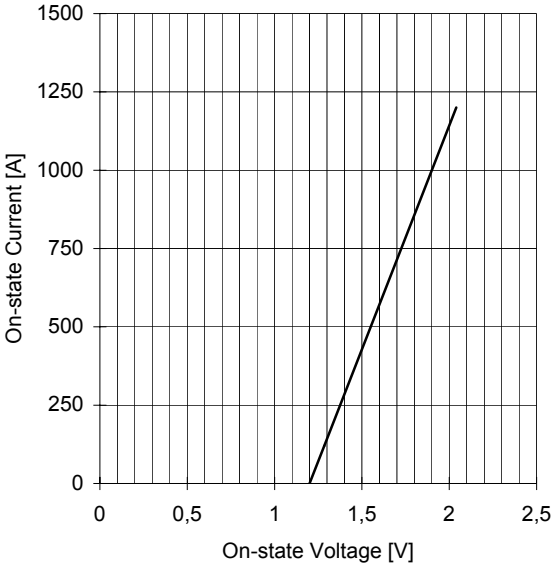
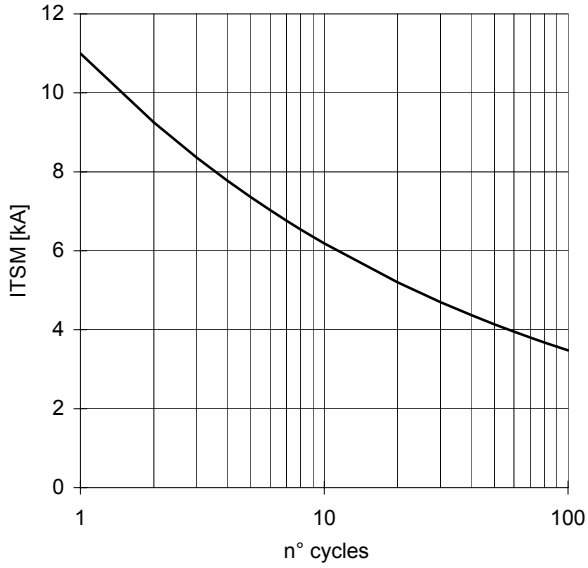
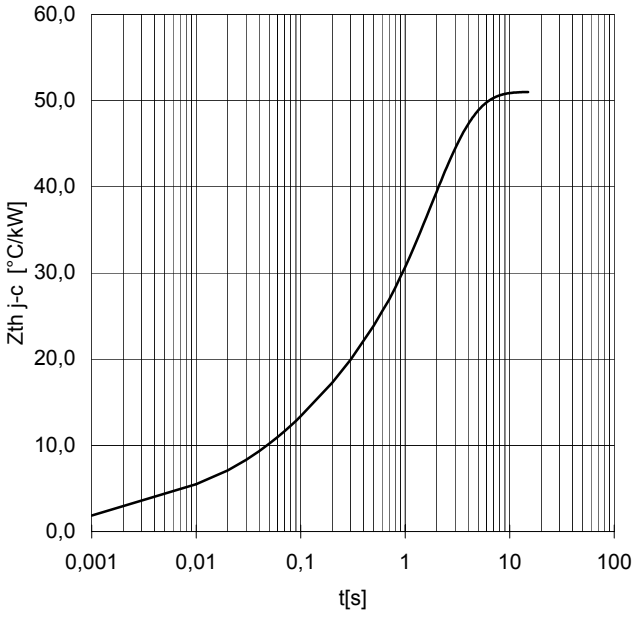
ON-STATE CHARACTERISTIC
Tj = 125 °C

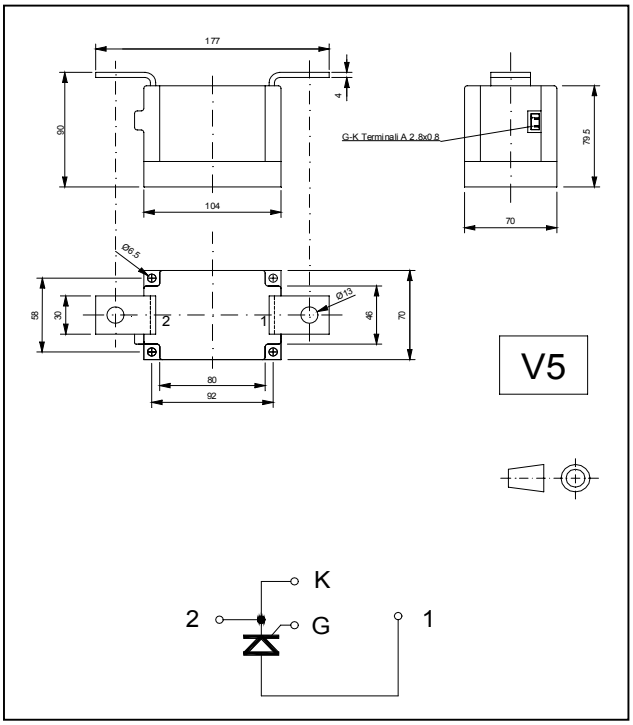


SURGE CHARACTERISTIC
Tj = 125 °C



TRANSIENT THERMAL IMPEDANCE





All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.
In the interest of product improvement POSEICO SPA reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

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