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## HIGH CURRENT PHASE CONTROL THYRISTOR INSULATED MODULE

- Full hermetic packaging
- Base plate insulation using AlN substrate
- Industrial compatible packaging
- Contract screws available on request

# AZT1150

Repetitive voltage up to **800 V**  
 Mean on-state current **1150 A**  
 Surge current **30 kA**

### TARGET SPECIFICATION

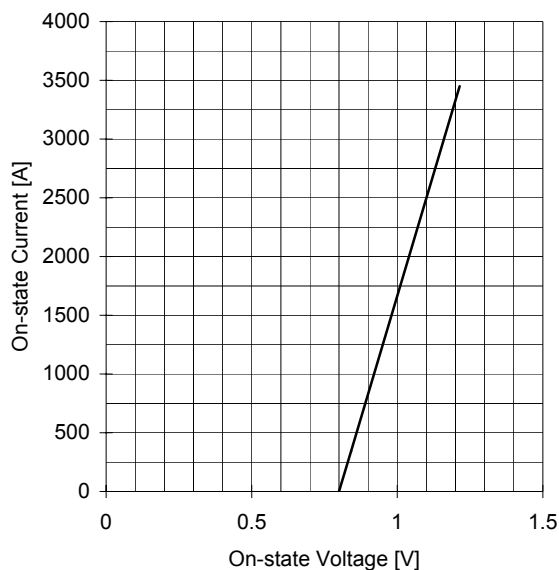
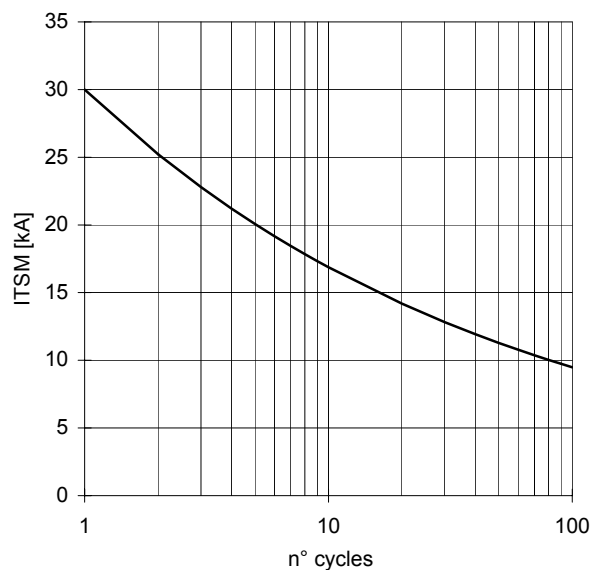
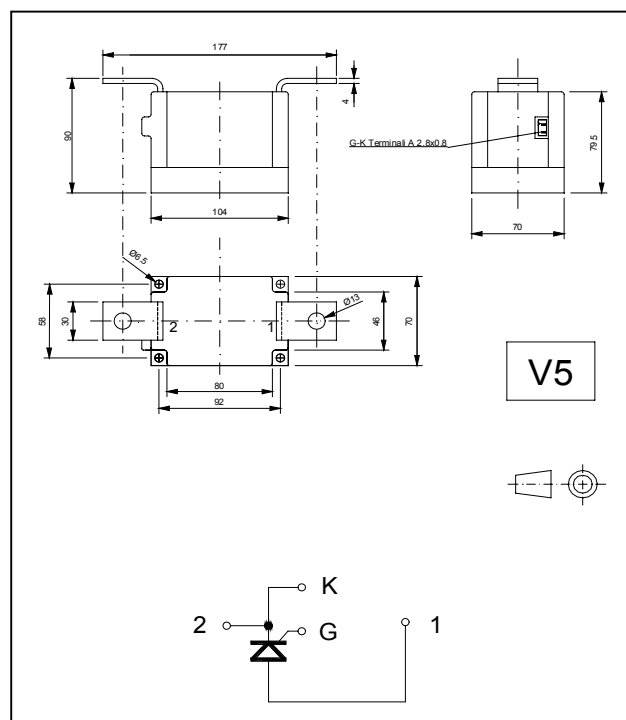
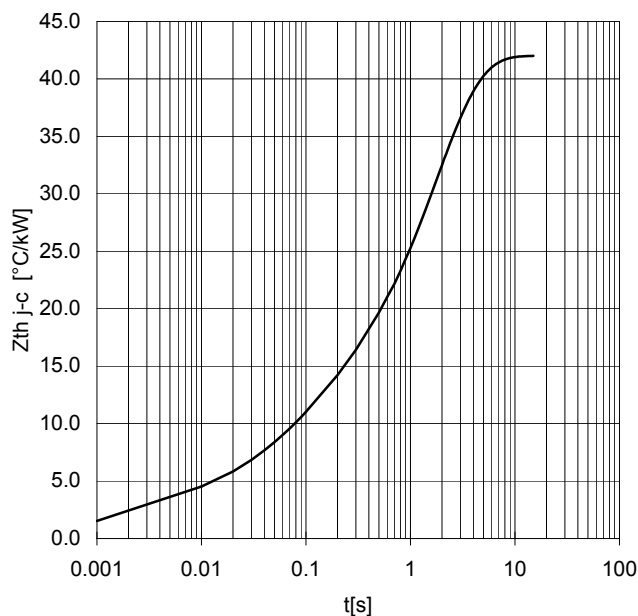
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Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit
<b>BLOCKING</b>					
V <sub>RRM/DRM</sub>	Repetitive peak reverse/off-state voltage		140	800	V
V <sub>RSM</sub>	Non-repetitive peak reverse voltage		140	900	V
I <sub>RRM/DRM</sub>	Repetitive peak reverse/off-state current		140	100	mA
<b>CONDUCTING</b>					
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50Hz, T <sub>c</sub> =85°C		1150	A
I <sub>T(AV)</sub>	Mean on-state current	180° sin. 50Hz, T <sub>c</sub> =55°C		1590	A
I <sub>TSM</sub>	Surge on-state current	sine wave, 10 ms	140	30	kA
I <sup>2</sup> t	I <sup>2</sup> t	without reverse voltage		4500 x1E3	A <sup>2</sup> s
V <sub>T</sub>	On-state voltage	On-state current = 1800 A	25	1.22	V
V <sub>T(TO)</sub>	Threshold voltage		140	0.80	V
r <sub>T</sub>	On-state slope resistance		140	0.120	mohm
<b>SWITCHING</b>					
di/dt	Critical rate of rise of on-state current, min.	From 75% V <sub>DRM</sub> up to 1050 A, gate 10V 5 ohm	140	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of V <sub>DRM</sub>	140	500	V/μs
t <sub>d</sub>	Gate controlled delay time, typical	V <sub>D</sub> = 100V, gate source 25 V, 10 ohm, tr = 0.5 μs	25	3	μs
t <sub>q</sub>	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 75% V <sub>DRM</sub>		250	μs
Q <sub>rr</sub>	Reverse recovery charge	di/dt = -20 A/μs, I = 700 A	140		μC
I <sub>rr</sub>	Peak reverse recovery current	V <sub>R</sub> = 50 V			A
I <sub>H</sub>	Holding current, typical	V <sub>D</sub> = 5V, gate open circuit	25	300	mA
I <sub>L</sub>	Latching current, typical	V <sub>D</sub> = 5 V, t <sub>p</sub> = 30 μs	25	700	mA
<b>GATE</b>					
V <sub>GT</sub>	Gate trigger voltage	V <sub>D</sub> = 5 V	25	3.5	V
I <sub>GT</sub>	Gate trigger current	V <sub>D</sub> = 5 V	25	300	mA
V <sub>GD</sub>	Non-trigger gate voltage, min.	V <sub>D</sub> = V <sub>DRM</sub>	140	0.25	V
V <sub>FGM</sub>	Peak gate voltage (forward)			30	V
I <sub>FGM</sub>	Peak gate current			10	A
V <sub>RGM</sub>	Peak gate voltage (reverse)			5	V
P <sub>GM</sub>	Peak gate power dissipation	Pulse width 100 μs		150	W
P <sub>G</sub>	Average gate power dissipation			2	W
<b>MOUNTING</b>					
R <sub>th(j-c)</sub>	Thermal impedance, DC	Junction to case		42	°C/kW
R <sub>th(c-h)</sub>	Thermal impedance	Case to heatsink		20	°C/kW
T <sub>j</sub>	Operating junction temperature			-30 / 140	°C
V <sub>ins</sub>	RMS insulation voltage	50Hz, circuit to base, all terminal shorted	25	4500	V
T	Mounting torque	Case to heatsink		4 to 6	Nm
	Mass			2800	g
<b>ORDERING INFORMATION : AZT1150 S 08</b> standard specification <input type="checkbox"/> <input type="checkbox"/> VDRM&VRRM/100					

**AZT1150****HIGH CURRENT PHASE CONTROL  
THYRISTOR INSULATED MODULE**

**POSEICO**  
 POSEICO SPA  
 Power Semiconductors Italian Corporation

TARGET SPECIFICATION feb 04 - ISSUE : 1

**ON-STATE CHARACTERISTIC**  
 $T_j = 140\text{ }^\circ\text{C}$ 

**SURGE CHARACTERISTIC**  
 $T_j = 140\text{ }^\circ\text{C}$ 

**TRANSIENT THERMAL IMPEDANCE**


All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < 0.03 mm and roughness < 2  $\mu\text{m}$ .

In the interest of product improvement POSEICO SPA reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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