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**PHASE CONTROL MODULE****ATT461**

- \*Full ermetic packaging
- \*Industrial compatible packaging
- \*Insulation using Aln substrate
- \*New G-K auxiliary output arrangement
- \*Contact screws available on request

Repetitive voltage up to **2400 V**  
Mean on-state current **460 A**  
Surge current **12 kA**

**FINAL SPECIFICATION SPECIFICATION**

mar 01 - ISSUE : 01

Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit
<b>BLOCKING</b>					
V <sub>RRM</sub> / DRM	Repetitive peak reverse/off-state voltage		125	2400	V
V <sub>RSM</sub>	Non-repetitive peak reverse voltage		125	2500	V
I <sub>RRM</sub> / DRM	Repetitive peak reverse/off-state current		125	50	mA
<b>CONDUCTING</b>					
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50Hz, T <sub>c</sub> =85°C		460	A
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50Hz, T <sub>c</sub> =55°C		680	A
I <sub>TSM</sub>	Surge on-state current	sine wave, 10 ms	125	12	kA
I <sup>2</sup> t	I <sup>2</sup> t	without reverse voltage		720 x1E3	A <sup>2</sup> s
V <sub>T</sub>	On-state voltage	On-state current = 1600 A	25	2	V
V <sub>T(TO)</sub>	Threshold voltage		125	1.1	V
r <sub>T</sub>	On-state slope resistance		125	0.552	mohm
<b>SWITCHING</b>					
di/dt	Critical rate of rise of on-state current, min.	From 75% VDRM up to 1050 A, gate 10V 5ohm	125	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	125	500	V/μs
td	Gate controlled delay time, typical	VD=100V, gate source 25V, 10 ohm , tr=.5 μs	25	1.1	μs
tq	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 75% VDRM		200	μs
Q <sub>rr</sub>	Reverse recovery charge	di/dt=-20 A/μs, I <sub>e</sub> = 700 A	125		μC
I <sub>rr</sub>	Peak reverse recovery current	VR= 50 V			A
I <sub>H</sub>	Holding current, typical	VD=5V, gate open circuit	25	300	mA
I <sub>L</sub>	Latching current, typical	VD=5V, tp=30μs	25	700	mA
<b>GATE</b>					
V <sub>GT</sub>	Gate trigger voltage	VD=5V	25	3.5	V
I <sub>GT</sub>	Gate trigger current	VD=5V	25	250	mA
V <sub>GD</sub>	Non-trigger gate voltage, min.	VD=VDRM	125	0.25	V
V <sub>FGM</sub>	Peak gate voltage (forward)			30	V
I <sub>FGM</sub>	Peak gate current			10	A
V <sub>RGM</sub>	Peak gate voltage (reverse)			5	V
P <sub>GM</sub>	Peak gate power dissipation	Pulse width 100 μs		150	W
P <sub>G</sub>	Average gate power dissipation			2	W
<b>MOUNTING</b>					
R <sub>th(j-c)</sub>	Thermal impedance	Junction to case, per element		50	°C/kW
R <sub>th(c-h)</sub>	Thermal impedance	Case to heatsink, per element		20	°C/kW
T <sub>j</sub>	Operating junction temperature			-30 / 125	°C
V <sub>ins</sub>	RMS insulation voltage	50Hz, circuit to base,all terminal shorted	25	4500	V
T	Mounting tourque	Case to heatsink		4 to 6	Nm
		Busbars to terminals		12 to 18	Nm
	Mass			1500	g
<b>ORDERING INFORMATION : ATT461 S 24</b>					
standard specification <input type="checkbox"/> <input type="checkbox"/> VDRM&VRRM/100					

# ATT461 PHASE CONTROL MODULE

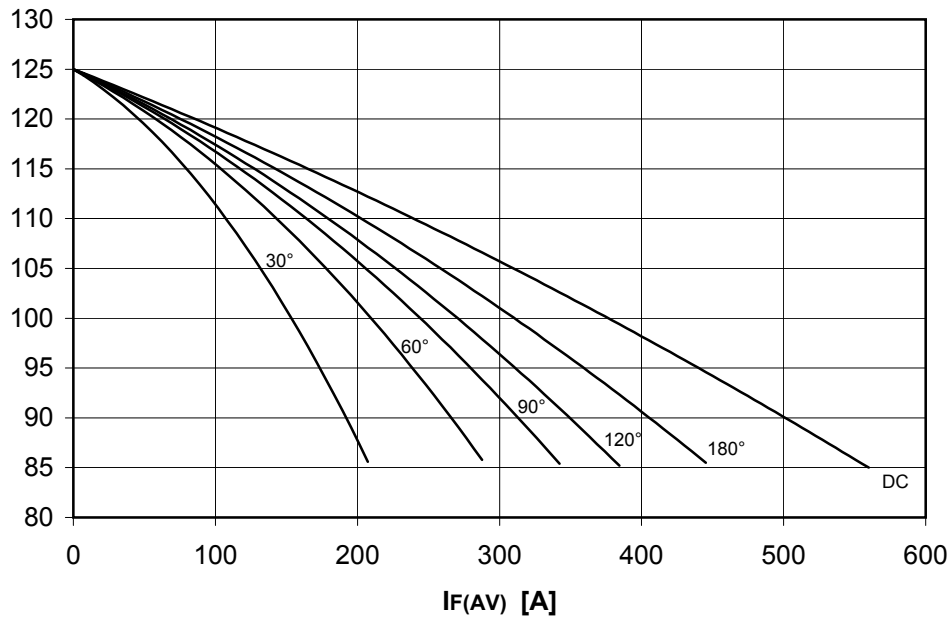


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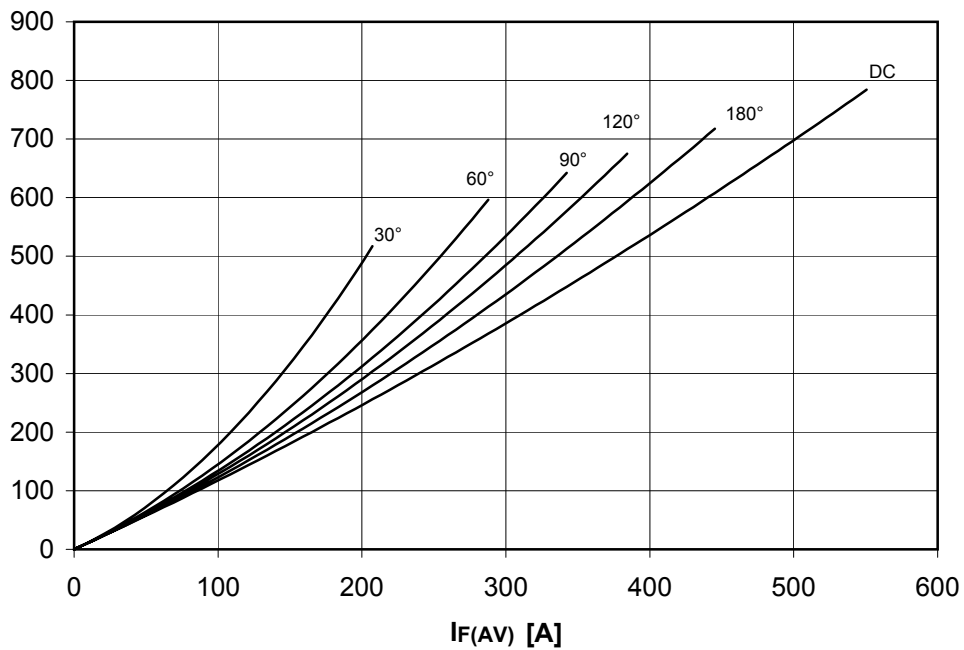
## DISSIPATION CHARACTERISTICS

### SQUARE WAVE

T<sub>case</sub> [°C]



P<sub>F(AV)</sub> [W]



# ATT461 PHASE CONTROL MODULE

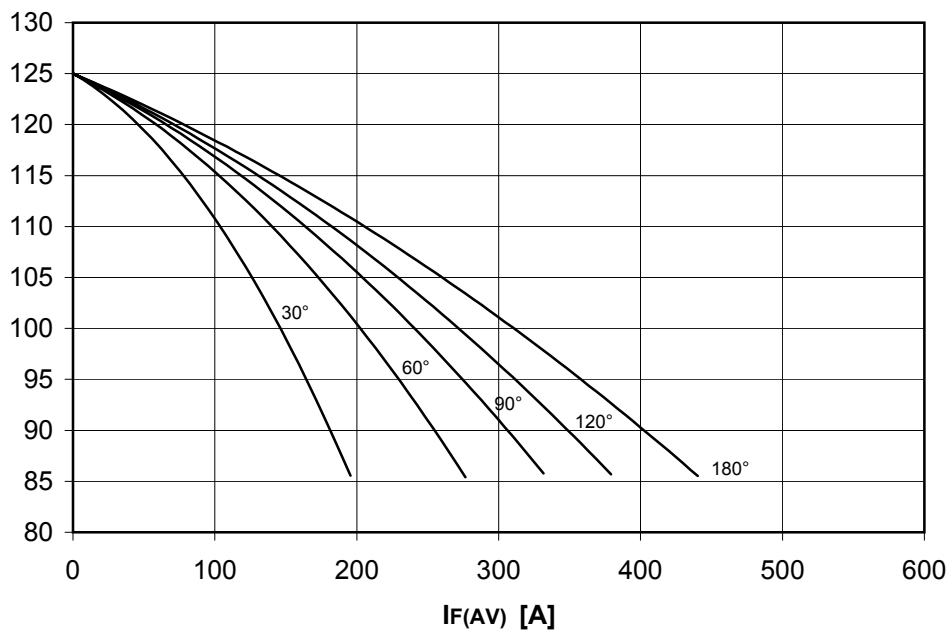


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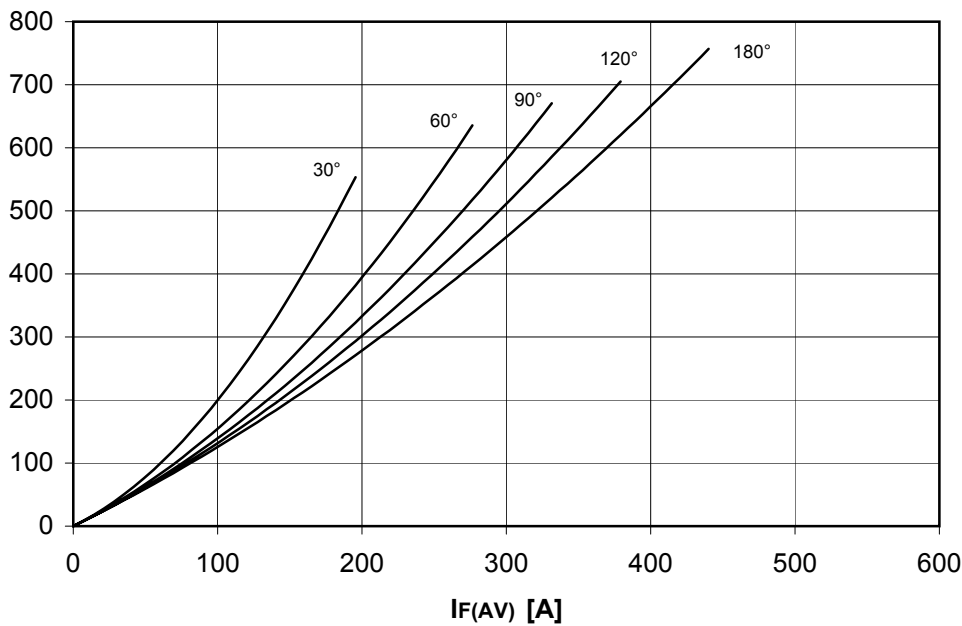
## DISSIPATION CHARACTERISTICS

SINE WAVE

$T_{case}$  [°C]



$P_{F(AV)}$  [W]

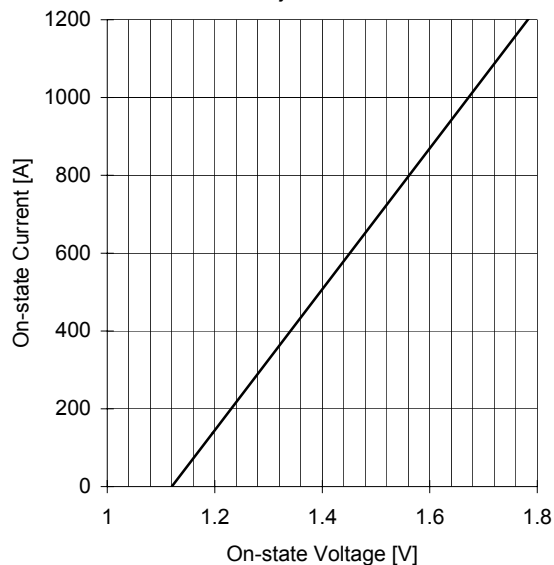


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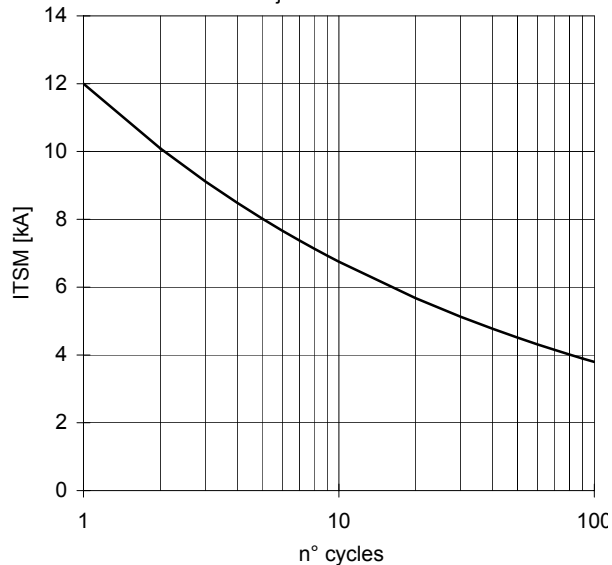


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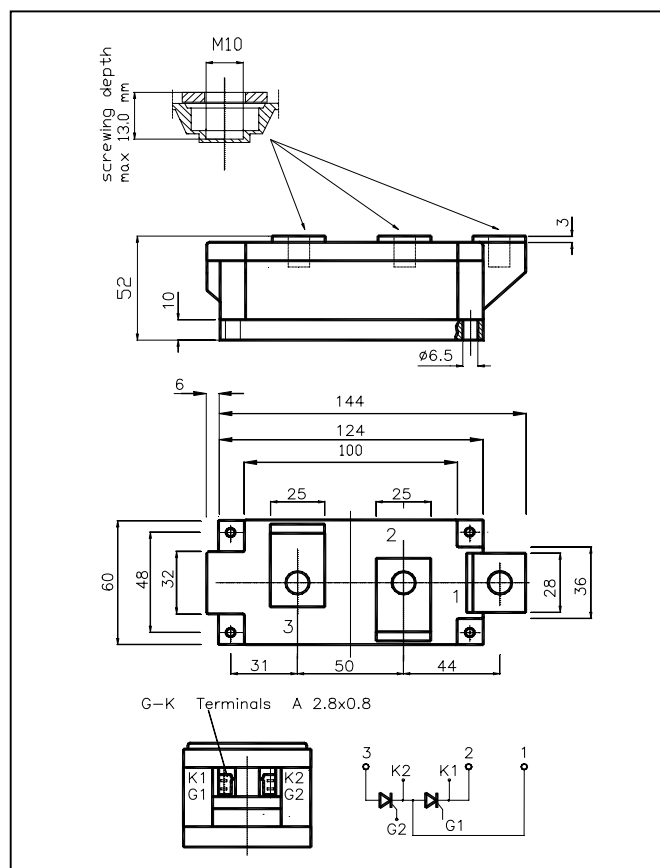
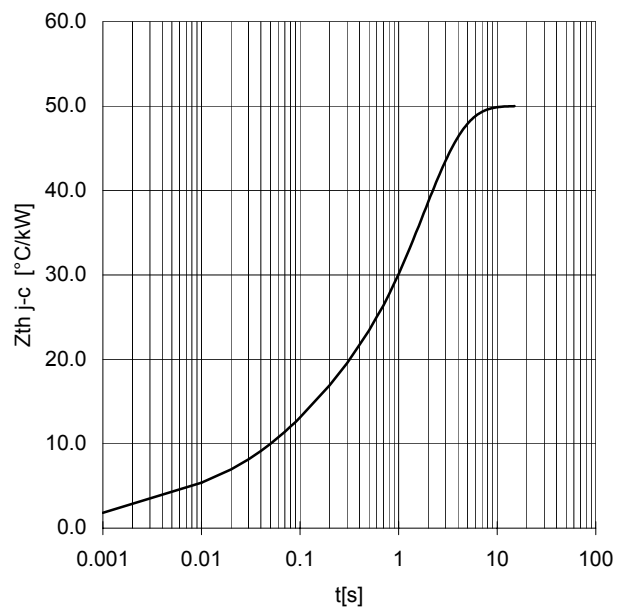
ON-STATE CHARACTERISTIC  
T<sub>j</sub> = 125 °C



SURGE CHARACTERISTIC  
T<sub>j</sub> = 125 °C



TRANSIENT THERMAL IMPEDANCE



All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 μm.  
In the interest of product improvement POSEICO SPA reserves the right to change any data given in this data sheet at any time without previous notice.  
If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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