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**PHASE CONTROL THYRISTOR****AT906**

Repetitive voltage up to

**800 V**

Mean on-state current

**5600 A**

Surge current

**95 kA****FINAL SPECIFICATION**

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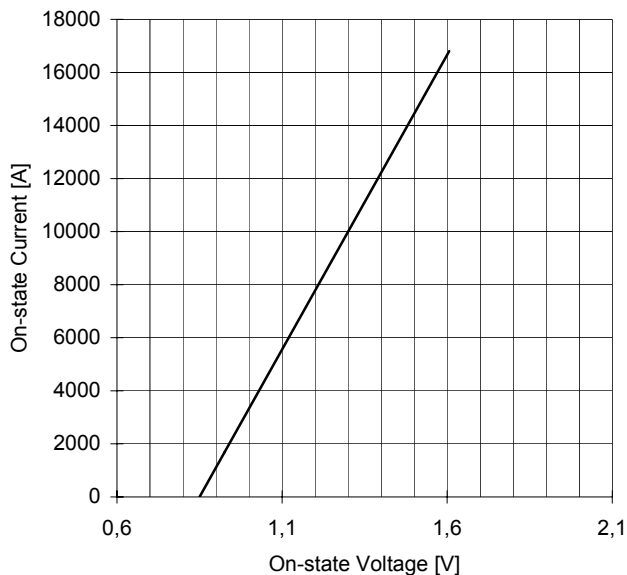
Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit
<b>BLOCKING</b>					
V <sub>RRM</sub>	Repetitive peak reverse voltage		125	800	V
V <sub>RSM</sub>	Non-repetitive peak reverse voltage		125	900	V
V <sub>DRM</sub>	Repetitive peak off-state voltage		125	800	V
I <sub>RRM</sub>	Repetitive peak reverse current	V=VRRM	125	300	mA
I <sub>DRM</sub>	Repetitive peak off-state current	V=VDRM	125	300	mA
<b>CONDUCTING</b>					
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		5600	A
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		4540	A
I <sub>TSM</sub>	Surge on-state current	sine wave, 10 ms	125	95	kA
I <sup>2</sup> t	I <sup>2</sup> t	V <sub>R</sub> ≤ 0.5 V <sub>RRM</sub>		45125 x1E3	A <sup>2</sup> s
V <sub>T</sub>	On-state voltage	On-state current = 9000 A	25	1,26	V
V <sub>T(TO)</sub>	Threshold voltage		125	0,85	V
r <sub>T</sub>	On-state slope resistance		125	0,045	mohm
<b>SWITCHING</b>					
di/dt	Critical rate of rise of on-state current, min.	From 75% V <sub>DRM</sub> up to 4000 A, gate 10V 5ohm	125	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of V <sub>DRM</sub>	125	1000	V/μs
td	Gate controlled delay time, typical	V <sub>D</sub> =100V, gate source 10V, 10 ohm, tr=.5 μs	25		μs
tq	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 75% V <sub>DRM</sub>		500	μs
Q <sub>rr</sub>	Reverse recovery charge	di/dt=-20 A/μs, I= 4000 A	125		μC
I <sub>rr</sub>	Peak reverse recovery current	V <sub>R</sub> = 50 V			A
I <sub>H</sub>	Holding current, typical	V <sub>D</sub> =5V, gate open circuit	25	500	mA
I <sub>L</sub>	Latching current, typical	V <sub>D</sub> =12V, tp=30μs	25	3000	mA
<b>GATE</b>					
V <sub>GT</sub>	Gate trigger voltage	V <sub>D</sub> =12V	25	3,5	V
I <sub>GT</sub>	Gate trigger current	V <sub>D</sub> =12V	25	400	mA
V <sub>GD</sub>	Non-trigger gate voltage, min.	V <sub>D</sub> =V <sub>DRM</sub>	125	0,4	V
V <sub>FGM</sub>	Peak gate voltage (forward)			30	V
I <sub>FGM</sub>	Peak gate current			10	A
V <sub>RGM</sub>	Peak gate voltage (reverse)			10	V
P <sub>GM</sub>	Peak gate power dissipation	Pulse width 100 μs		150	W
P <sub>G</sub>	Average gate power dissipation			3	W
<b>MOUNTING</b>					
R <sub>th(j-h)</sub>	Thermal impedance, DC	Junction to heatsink, double side cooled		8,5	°C/kW
R <sub>th(c-h)</sub>	Thermal impedance	Case to heatsink, double side cooled		2	°C/kW
T <sub>j</sub>	Operating junction temperature			-30 / 125	°C
F	Mounting force			80 / 100	kN
	Mass			3000	g
<b>ORDERING INFORMATION : AT906 S 08</b>					
standard specification <input type="checkbox"/> VDRM&VRRM/100 <input type="checkbox"/>					

# AT906 PHASE CONTROL THYRISTOR

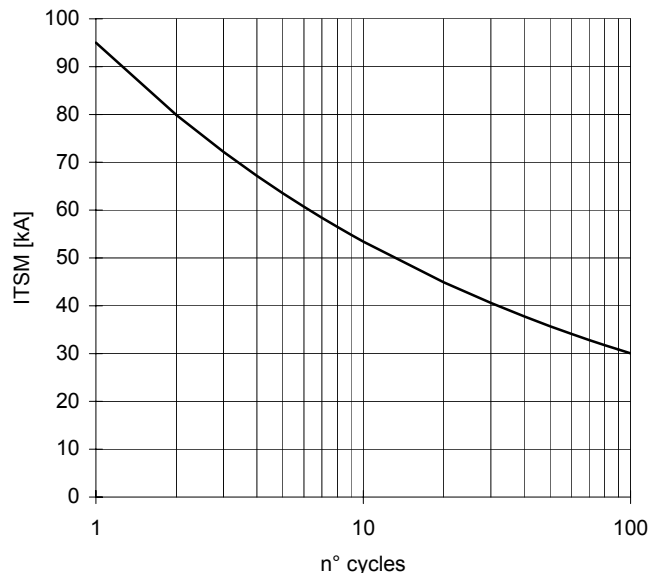


FINAL SPECIFICATION dic 03 - ISSUE : 2

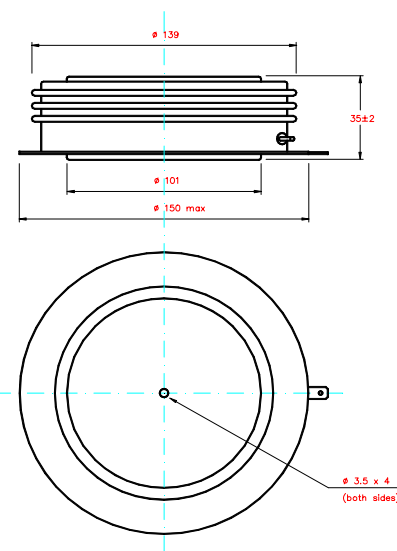
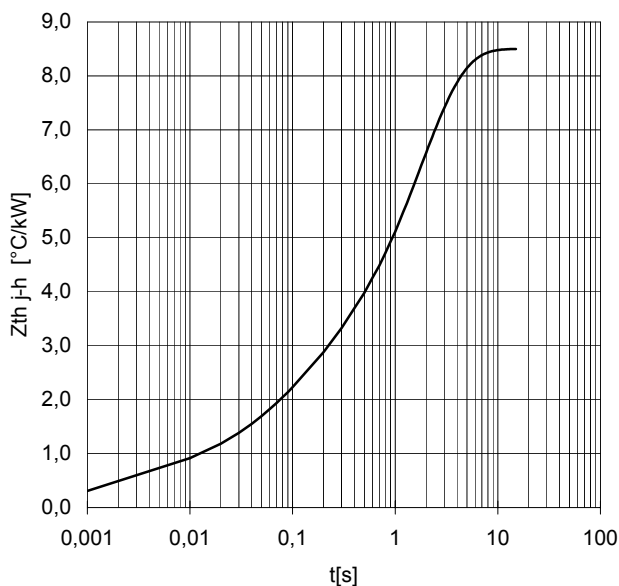
ON-STATE CHARACTERISTIC  
 $T_j = 125\text{ }^\circ\text{C}$



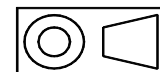
SURGE CHARACTERISTIC  
 $T_j = 125\text{ }^\circ\text{C}$



TRANSIENT THERMAL IMPEDANCE  
DOUBLE SIDE COOLED



Dimensions  
in mm



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

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All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness <math>< .03\text{ mm}</math> and roughness <math>< 2\text{ }\mu\text{m}</math>.

In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.