Introduction

As the first isolated power module on the world SEMIPACK 1 was invented in 1975 by SEMIKRON. Now SEMIPACK has already become a complete family with different case sizes and configurations. SEMIPACK products have the widest output current range up to 1200 A, reverse voltage from 600V to 2200V. At present, there are three production locations for SEMIPACK products: SKSK (Slovakia), aimed at soldered and bonded modules; SKCNP (China) specializes in pressure contact modules and SKI (Italy), which manufactures fast diode modules and special types.

Features

Semiconductor chips soldered onto ceramic isolated metal baseplate (SEMIPACK 0…2 and some SEMIPACK 3 modules) or pressure contact modules (SEMIPACK 3,4,5,6) with very high load cycle capability.

SEMIPACK products consist of thyristor modules, rectifier diode modules and fast diode modules. The respondent current rating and voltage class is given below:

- For thyristor modules: current rating is from 15A to 800A, voltage class is from 600V to 2200V.
- For rectifier diode modules: current rating is from 15A to 1200A, voltage class is from 600V to 2200V.
- For fast diode modules: current rating is from 40A to 205A, voltage class is from 400V to 1700V.

Optimum heat transfer to heat sink thanks to ceramic isolated metal baseplate with Al_3O_2 (SEMIPACK 0,1,2) or AIN (SEMIPACK 3,4,5,6) Insolating substrate and copper baseplate.

Thyristor chips in SEMIPACK 3…6 with amplifying gate to reduce the gate current

Fast diode modules with diodes in diffusion, Epitaxial and CAL (Controlled Axial Lifetime) technology up to 600 A and 1700 V.

UL recognized; file no. E 63 532

Housings of SEMIPACK

Fig.1 SEMIPACK products family

SEMIPACK has 7 different housing sizes, from SEMIPACK 0 to SEMIPACK 6. Below are mean dimensions of different housings:

Case	Length (mm)	Width (mm)	Height (mm)
SEMIPACK 0	61	21	23.2
SEMIPACK 1	93	20	30
SEMIPACK 2	94	29	30
SEMIPACK 3	115	51	52
SEMIPACK 4	101	50	52
SEMIPACK 5	150	60	52
SEMIPACK 6	140	70	90

Fig. 2 Main dimensions of different SEMIPACK housing sizes

For SEMIPACK products, standard tolerance of catalogue drawings is +/-0.5mm.

Mounting/Assembly Instructions

Preparation, surface specifications

In order to ensure good thermal contact and to obtain the thermal contact resistance values specified in the datasheets, the contact surface of the heat sink must be clean and free from dust particles, as well as fulfilling the following mechanical specifications:

unevenness: < 50µm over a distance of 100 mm

Roughness Rz: < 10µm

Before assembly onto the heat sin, the module baseplate or the contact surface of the heat sink is to be evenly coated with a thin layer (approx. 50µm) of a thermal compound such as Wacker- Chimie P12.

For even distribution we recommend using a hard rubber roller or a silk screen process.

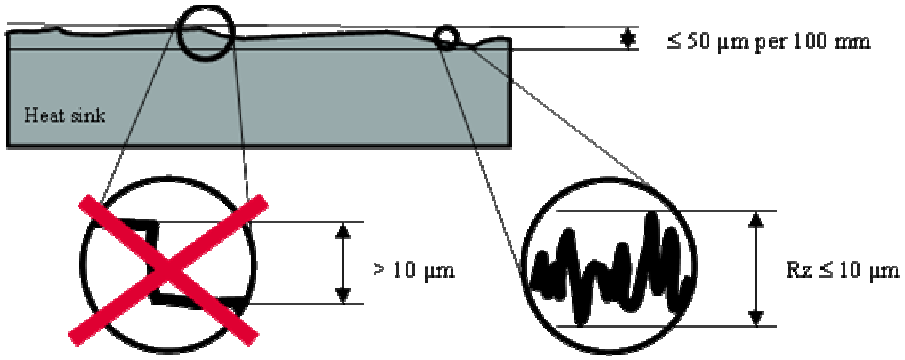

Fig.1 Heat sink surface specifications

Applying Thermal Paste

A thin layer of thermal paste has to be applied onto the heat sink surface or the underside of the module. A layer thickness of 50 µm – 100 µm is recommended for Silicone Paste P 12 from WACKER CHEMIE.

The thickness of the layer can be determined using a measurement gauge as shown in Fig.9.2

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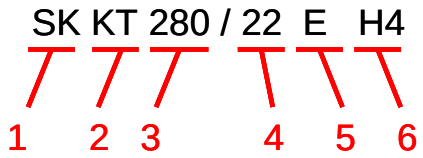
Fig.2 Wet film thickness gauge 5-150 µm

SEMIKRON recommends using screen printing to apply thermal paste. In certain cases a hard rubber roller might be suitable for the application of thermal paste.

Type Designation

Type designation



1: SEMIKRON compenent

2: Topology of internal connection, pls refer to *Fig.1-2*

3: Rated current (I_{TAV} [A])

4: Voltage class (V_{RRM}[V])

5: dv/dt class5

D: 500 V/μs

E: 1000 V/μs

G: 2000 V/μs

6: Option, where applicable, e.g. H4= Visol 4.8 kV/1s

Topologies

SEMPACK products are available as single component elements or double packs with internal, functional interconnection. 10 available tologies are given as below:

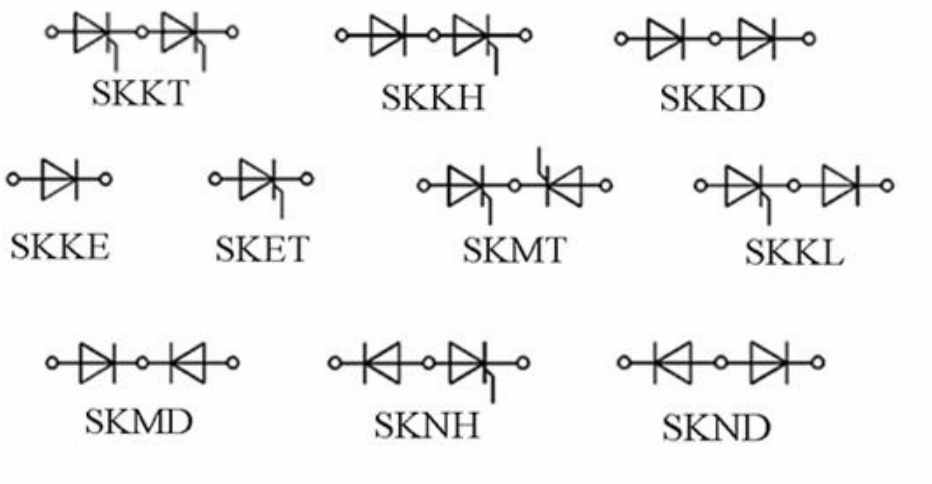


Fig.1 SEMIPACK available topologies

Technical Details

- **Data sheet captions Explanations of data sheet values**

Explanation of electrical parameters

The terms in [ ] apply to thyristors only

Insulation voltage V_{isol}

The insulation voltage of SEMIPACK® modules is a guaranteed value for the insulation between the terminals and the base plate. The limiting value 3.6 kV_{rms} specified for 1 s subject to 100 % production testing.

All terminals - including the gate connections - must be interconnected during dielectric testing. All specifications for the final product's dielectric test voltage are described in the IEC publications IEC 60146-1-1: 1991 and EN 60146-1-1: 1994 Section 4.2.1 (=VDE 0558 T1-1: 1993), EN 50 178: 11.1997 (= DIN EN 50 178 (VDE 0160): 1998, as well as in UL 1557: 1997. For railway applications, for instance, please refer to the specifications of the IEC 61287-1 standard.

Non-repetitive peak reverse voltage V_{RSM}; [Non-repetitive peak off-state voltage V_{DSM}] Maximum permissible value for non-repetitive, occasionally transient peak voltages.

Repetitive peak reverse and off-state voltages [V_{DRM}] and V_{RRM} Maximum permissible value for repetitive transient off-state and reverse voltages.

Direct reverse voltages V_R for continuous duty Maximum permissible direct reverse voltage for stationary operation for diodes (V_R) [or thyristors (V_D, V_R)]. This value is 0.7 V_{RRM} [0.7 V_{DRM}].

Mean forward [on-state] current I_{FAV}, [I_{TAV}] The symbols I_{FAV}, [I_{TAV}] are used to refer to both the mean current values in general and the current limits. The limiting values are absolute maximum continuous values for the on-state current load of a diode [thyristor] for a given current waveform and given cooling conditions (e.g. case temperature T_c). At this current value, the maximum permissible junction temperature is reached, with no margins for overload or worst-case reserves. The recommended maximum continuous current is therefore approximately 0.8 I_{TAV} . For operation frequencies of between 40 Hz and 200 Hz the maximum mean on-state current can be taken from Fig. 1 of the datasheet. If standard diodes and thyristors

(diodes/thyristors for line application) are operated at frequencies of between 200 Hz and 500 Hz, further current reduction should be carried out to compensate for the switching losses that are no longer negligible.

RMS forward [on-state] current I_{FRMS}, [I_{TRMS}]

The symbols I_{FRMS}, [I_{TRMS}] are used to refer to both the mean current values and the current limits. The limiting values are absolute maximum values for the continuous on-state current for any chosen current waveform and cooling conditions.

Surge forward [on-state] current I_{FSM} [I_{TSM}]

Crest value for a surge current in the form of a single sinusoidal half wave which lasts for 10 ms. After occasional current surges with current values up to the given surge forward current, the diode [thyristor] can withstand the reverse voltages specified in Fig. 8 or Fig. 16 of the datasheets.

Surge current characteristics $I_{F(OV)}$, [$I_{T(OV)}$]

Crest values for full or part sinusoidal half wave currents lasting between 1 ms and 10 ms or for sequential sinusoidal half wave currents with a maximum duration of 10 ms, permissible under fault conditions only, i.e. the diode [thyristor] may only be subjected to this value occasionally; the controllability of a thyristor may be lost during overload. The overload current depends on the off-state voltage value across the component (cf. Fig. 8 or Fig. 16 of the datasheets).

i^2t value

This value is given to assist in the selection of suitable fuses to provide protection against damage caused by short circuits and is given for junction temperatures of 25 ℃ and 125 ℃. The i^2t value of the fuse for the intended input voltage and the prospective short circuit in the device must be lower than the i^2t of the diode [thyristor] for t = 10 ms. When the operating temperature increases, the i^2t value of the fuse falls more rapidly than the i^2t value of the diode [thyristor], a comparison between the i^2t of the diode (thyristor) for 25 ℃ and the i^2t value of the (unloaded) fuse is generally sufficient.

The i^2t value is calculated from the surge on-state current I_{TSM} using the equation:

$$\int_0^{t_{hw}} i_{TS}^2 dt = I_{TSM}^2 \cdot \frac{t_{hw}}{2}$$

t_{hw} is the duration of the half sinewave for which I_{TSM} has been specified. Thus at 50 Hz $t_{hw}/2$ = 0,005 s. i^2t has practically the same value for 60 as for 50 Hz since the 10% higher I_{TSM} is balanced out by the lower value for t_{hw} : $1.1^2 \cdot 8.3 \approx 10$.

[Critical rate of rise of on-state current $(di/dt)_{cr}$]

Immediately after the thyristor has been triggered, only part of the chips conducts the current flow, meaning that the rate rise of the on-state current has to be limited. The critical values specified apply to the following conditions: repetitive loads of between 50 and 60 Hz; a peak current value corresponding to the crest value of the permissible on-state current for sinusoidal half waves; a gate trigger current that is five times the peak trigger current with a rate of rise of at least 1 A/µs. The critical rate of rise for on-state current falls as the frequency increases, but rises as the peak on-state current decreases. For this reason, for frequencies > 60 Hz and pulses with a high rate of rise of current, the peak on-state current must be reduced to values below those given in the datasheets.

[Critical rate of rise of off-state voltage $(dv/dt)_{cr}$]

The values specified apply to an exponential increase in off-state voltage to 0.66 V_{DRM}. If these values are exceeded, the thyristor can break over and self trigger.

Direct reverse [off-state] current I_{RD} [I_{DD}]

Maximum reverse or off-state [for thyristors] current for the given temperature and maximum voltage. This value depends exponentially on the temperature.

Direct forward [on-state] voltage V_F [V_T]

Maximum forward voltage across the main terminals for a given current at 25 ℃.

Threshold voltage $V_{(TO)}$ [$V_{T(TO)}$] and Forward [on-state] slope resistance r_T

These two values define the forward characteristics (upper value limit) and are used to calculate the instantaneous value of the forward power dissipation P_F [P_T] or the mean forward power dissipation P_{FAV} [P_{TAV}]:

$P_{F[T]} = V_{T(TO)} * I_{F[T]} + r_T * i^2_{F[T]}$

$P_{F[T]AV} = V_{T(TO)} * I_{F[T]AV} + r_T * I^2_{F[T]RMS}$

$I^2_{F[T]RMS} / I^2_{F[T]AV} = 360° / \Theta$

for square-wave pulses

$I^2_{F[T]RMS} / I^2_{F[T]AV} = 2.5$ or

$I^2_{F[T]RMS} / I^2_{F[T]AV} = (\pi/2)^2 * 180° / \Theta$

for [part] sinusoidal half waves

Θ: Current flow angle

$i_{F[T]}$: Instantaneous forward current value

$I_{F[T]RMS}$: RMS forward [on-state] current

$I_{F[T]AV}$: Mean forward [on-state] current

[Latching current I_L]

Minimum anode current which at the end of a triggering pulse lasting 10 µs will hold the thyristor in its on-state. The values specified apply to the triggering conditions stipulated in the section on "Critical rate of rise of on-state current".

[Holding current I_H]

Minimum anode current which will hold the thyristor in its on-state at a temperature of 25 ℃. If the thyristor is switched on at temperatu res below 25 ℃, the values specified may be exceeded.

Recovery charge Q_{rr}

Q_{rr} is the total charge which flows through the main circuit (current-time area) during commutation against the reverse recovery time t_{rr}. The corresponding characteristic in the datasheet shows this value's dependence on the forward current threshold value I_{FM} [I_{TM}] before commutation, as well as the forward current rate of fall di/dt (cf. Fig. 1).

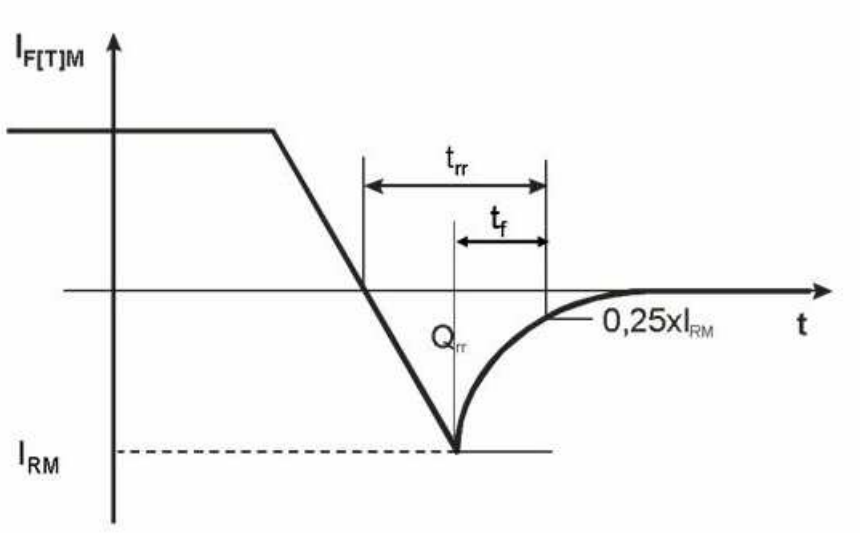


Fig. 1 Current curve during diode/thyristor turn-off

The following relations exist between t_{rr}, Q_{rr}, the current fall time t_f and the peak reverse recovery current I_{RM} (cf. Fig. 1):

$t_{rr} = I_{RM} / (- di_{F[T]}/dt) + t_f$

$t_{rr} = SQR (2 * Q_{rr} / (- di_{F[T]}/dt) + t_f^2 / 4) + t_f / 2$

$I_{RM} = 2 * Q_{rr} / t_{rr}$

$I_{RM} = SQR (2 * Q_{rr} * (- di_{F[T]}/dt) + t_f^2 / 4 * (- di_{F[T]}/dt)^2) - t_f / 2 * (- di_{F[T]}/dt)$

If the fall rate of the forward current I_F [I_T] is very low, t_f will be small in comparison to t_{rr} and the equations can be simplified as follows:

$t_{rr} = SQR (2 * Q_{rr} / (- di_{F[T]}/dt))$

$I_{RM} = SQR (2 * Q_{rr} * (- di_{F[T]}/dt))$

Further details, in particular with regard to fast diode switching, can be found in the section "Fast rectifier diodes" under "Diode turn-off".

[Circuit commutated turn-off time t_q]

The circuit commutated turn-off time lies in the range of several hundred µs and constitutes the time required for a thyristor to discharge to allow it to take on forward

voltage again. This value is defined as the time that elapses between zero crossing of the commutation voltage and the earliest possible load with off-state voltage. In the case of thyristors for phase-commutated converters and a.c. converters, the circuit commutated turn-off time is usually of no significance. For this reason, the datasheets contain typical values only, and no guarantee is given for these values.

[Gate trigger voltage V_{GT} and Gate trigger current I_{GT}]

Minimum values for square-wave triggering pulses lasting longer than 100 µs or for d.c. with 6 V applied to the main terminals. These values will increase if the triggering pulses last for less than 100 µs. For 10 µs, for instance, the gate trigger current I_{GT} would increase by a factor of between 1.4 and 2. Firing circuits should therefore be arranged in such as way that trigger current values are 4 to 5 times larger than I_{GT}. If the thyristor is loaded with reverse blocking voltage, no trigger voltage may be applied to the gate in order to in order to avoid a non-permissible increase in off-state power losses and the formation of hot spots on the thyristor chip.

[Gate non-trigger voltage V_{GD} und Non-trigger current I_{GD}]

These trigger voltage and current values will not cause the thyristor to fire within the permissible operating temperature range. Inductive or capacitive interference in the triggering circuits must be kept below these values.

[Time definitions for triggering]

Fig. 2 shows the characteristics of gate trigger signal V_G and anode-cathode voltage V_{AK} which define the time intervals for the triggering process.

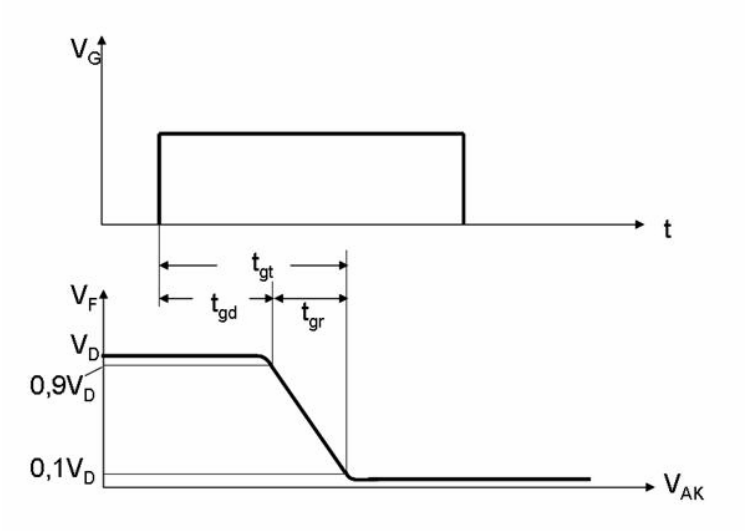


Fig. 2 Time definitions for thyristor triggering

[Gate-controlled delay time t_{gd}]: Time interval between the start of a triggering pulse and the point at which the anode-cathode voltage falls to 90 % of its starting value. The datasheet specifies a typical value which is applicable, provided the following conditions are fulfilled:

- Square-wave gate pulse, duration 100 µs

- Anode-cathode starting voltage 0.5 V_{DRM}

- On-state current after firing approx. 0.1 I_{TAV} @ 85 ℃

- Junction temperature during firing approx. 25 ℃

[Gate controlled rise time t_{gr}]: Period within which the anode-cathode voltage falls from 90 % to 10 % of its starting value during firing.

[Gate current pulse duration t_{gt}]: The sum of the gate controlled delay time t_{gd} and the gate controlled rise time t_{gr}.

Thermal resistances $R_{th(x-y)}$ and thermal impedances $Z_{th(x-y)}$

For SEMIPACK® modules, thermal resistances/impedances are given for the heat flow between points "x" and "y". The indices uses are as follows:

j - junction

c - case/base plate

s - sink

r - reference point

a - ambient

The contact thermal resistance case to heat sink $R_{th(c-s)}$ applies provided the assembly instructions are followed. In such cases, the given dependences of the internal thermal resistance junction to case $R_{th(j-c)}$ on the current waveform and the current flow angle should take into account any deviations from the maximum instantaneous value of the mean junction temperature calculated. The values given in the datasheet tables apply to sinusoidal half waves only. Values for other current waveforms can be taken from Fig. 7 of the datasheet.

The thermal resistance junction to ambient $R_{th(j-a)}$ to be used in Fig. 1 and Fig.11 of the datasheet comprises the following components:

$$\mathbf{R_{th(j-a)} = R_{th(j-c)} + R_{th(c-s)} + N * R_{th(h-a)}}$$

where N: the number of thyristors or diodes operating simultaneously on one heat sink.

The thermal resistance $R_{th(h-a)}$ of the heat sink decreases as the following items increase: power dissipation, the cooling air flow rate, the number of SEMIPACK® modules mounted and the distance between the individual modules.

The transient thermal impedances in the SEMIPACK® modules $Z_{th(j-c)}$ and $Z_{th(j-s)}$ are shown in the diagrams shown in Fig. 6 and Fig 14 of the datasheets as a function of the time t. For times > 1 s, the transient thermal impedance $Z_{th(s-a)}$ of the heat sink must be added to this in order to calculate the total thermal impedance. For this purpose, the datasheets for SEMIKRON heat sinks normally contain a diagram illustrating the given thermal impedance $Z_{th(s-a)}$ or $Z_{th(c-a)}$ as a function of the time t. When several components are being mounted on one heat sink, in order to calculate

the transient thermal impedance of one component, the thermal heat sink impedance must be multiplied by the total number of components N.

Temperatures

The most important referential value for calculating limiting values is the maximum permissible virtual junction temperature T_{vj}. At most in the event of a circuit fault (e.g. when a fuse is activated) may this value be exceeded briefly (cf. "Surge on-state current"). Another important reference point for the permissible current capability is the case temperature T_c. In SEMIPACK® modules, the measuring point for T_c (Reference point/Reference temperature T_{cref}) is the hottest point of the baseplate beneath the hottest chip, measured through a hole in the heat sink. The heat sink temperature T_s is of particular interest for defining power dissipation and heat sink. In SEMIPACK® modules the measuring point for T_s (Reference point/Reference temperature T_{sref}) is the hottest point of the heat sink besides the baseplate, measured from above on the side wall of the module (cf. also IEC 60747-1, Am. 1 to Am. 3 and IEC 60747-15 cls.7.4.3).
The permissible ambient conditions without current or voltage stress are described, among other things, by the maximum permissible storage temperature T_{stg}. The parameter T_{stg} is also the maximum permissible case temperature which must not be exceeded as a result of internal or external temperature rise.

Mechanical limiting values

The limiting values for mechanical load are specified in the datasheets, e.g.:

Mn : Max. tightening torque for terminal screws and fasteners

Ft : Max. permissible mounting force (pressure force) for capsule devices

a : Max. permissible amplitude of vibration or shock acceleration in x, y and z direction.

If SEMIPACK® modules with no hard mould are to be used in rotating applications, the soft mould mass may come away and leak. In such cases, Please contact SEMIKRON for there applications.

- R_{th}, $I_{T(F)MS}$, etc.

Measuring Thermal Resistance $R_{th(j-c)}$ and $R_{th(c-s)}$

The definition for thermal resistance R_{th} is the difference between two defined temperatures divided by the power loss P which gives rise to the temperature difference under steady state conditions:

$$R_{th(1-2)} = \frac{\Delta T}{P_V} = \frac{T_1 - T_2}{P_V} \qquad (1)$$

Depending upon the choice of the two temperatures the following thermal resistances can be distinguished:

- thermal resistance junction to case $R_{th(j-c)}$,

- thermal resistance case to heatsink $R_{th(c-s)}$,

- thermal resistance heatsink to ambient $R_{th(s-a)}$,

- thermal resistance junction to ambient $R_{th(j-a)}$, etc.

The data sheet values for the thermal resistances are based on measured values. As can be seen in equation (1), the temperature difference ΔT has a major influence on the R_{th} value. As a result, the reference points and the measurement methods will have a major influence too.

SEMIKRON measures the $R_{th(j-c)}$ and $R_{th(c-s)}$ using method A shown in *Fig.1*. This means the reference points are as follows:

- For $R_{th(j-c)}$ they are a virtual junction of the chip (T_j) and the bottom side of the module (T_c), measured directly underneath the chip via a drill hole in the heat sink. Reference point 1 in *Fig.1*.
- For $R_{th(c-s)}$ once again the bottom side of the module (T_c), measured as described above. The heat sink temperature T_s is measured on the top of the heat sink surface as close to the chip as possible.

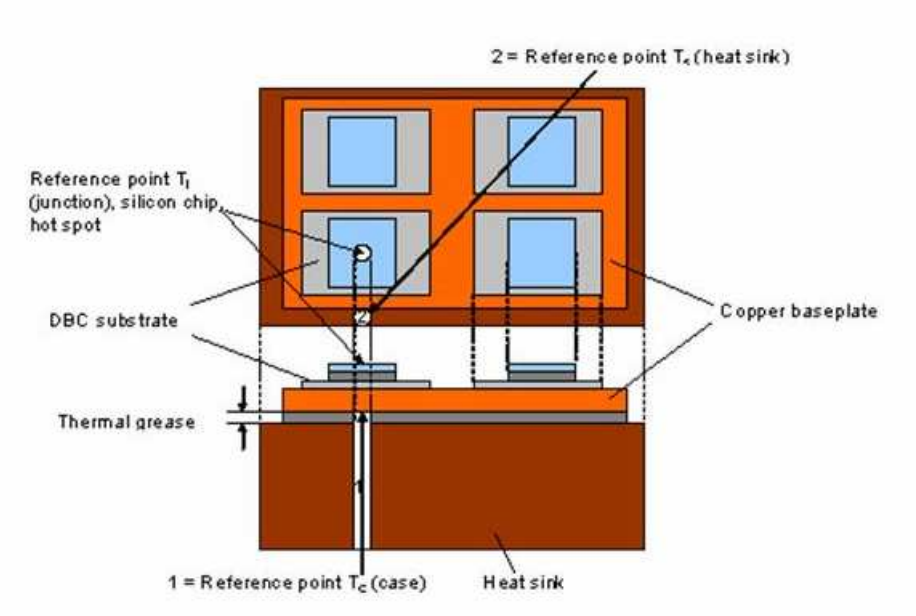


Fig.1 Method A as used for SEMIPACK, location of reference points for R_{th} measurement

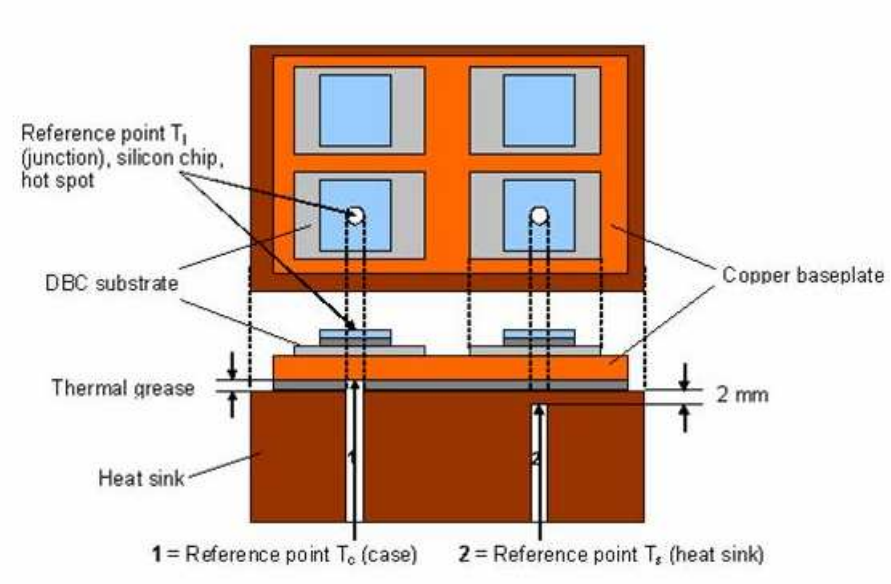


Fig.2 Method B, location of reference points for R_{th} measurement

As explained above, the measurement method and the reference points have a significant influence on the R_{th} value. Some competitors use method B, as shown in *Fig.2*. The main difference is the second reference point for the measurement of $R_{th(c-s)}$. See reference point 2 in *Fig.2.* This reference point is very close to the bottom side of the module inside the heat sink, i.e. in a drill hole. Due to the temperature

distribution inside the heat sink (as shown in *Fig.3*), the temperature difference ΔT (= T_c-T_s) is very small, meaning that $R_{th(c-s)}$ will be very small, too.

Fig.3 shows the temperature distribution and the location of the reference points for the different measurement methods. If equation (1) is taken into consideration, it is clear that $R_{th(c-s)}$ in method B must be smaller. That said, the reduction in $R_{th(c-s)}$ must ultimately be added to $R_{th(s-a)}$ (see *Fig.4*), meaning that at least the thermal resistance $R_{th(j-a)}$ between junction and the ambient turns out to be the same, regardless of what measurement method is used.

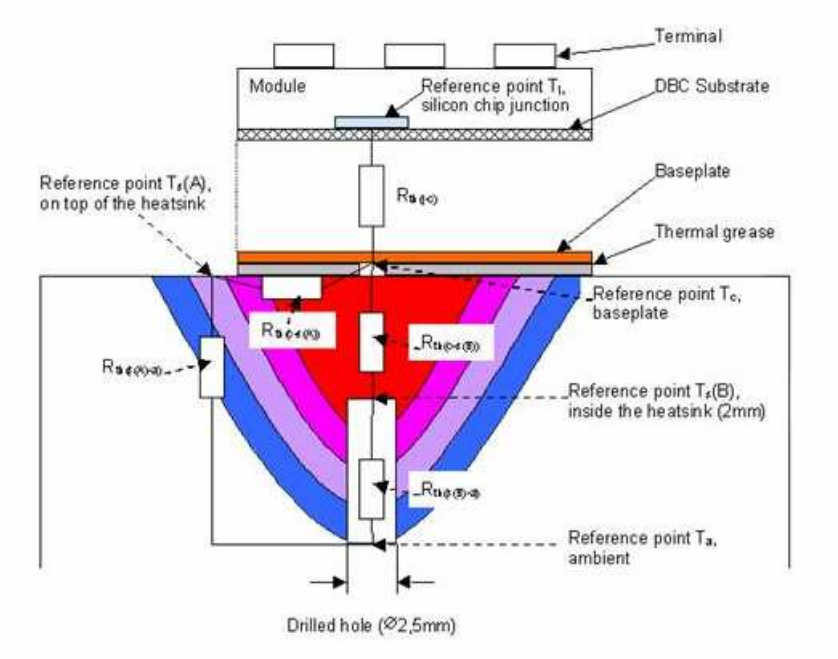


Fig.3 Thermao distribution and positions of different reference points for Tj, Tc, Ts and Ta for the methodes A and B

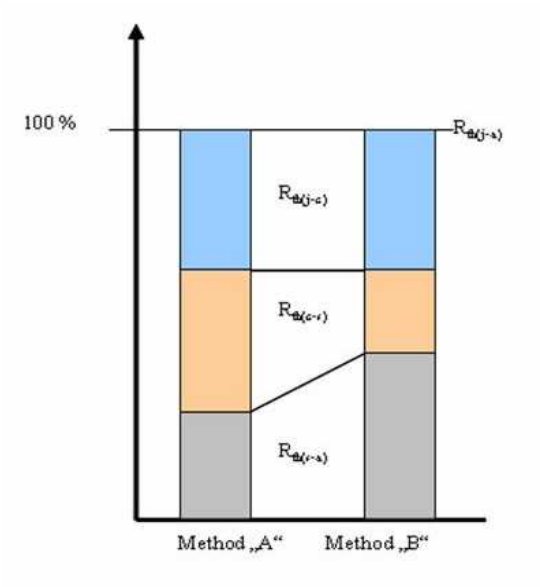


Fig.4 Comparison of the resulting Rth values for the different methods

For further information on the measurement of thermal resistances please refer to:

- M. Freyberg, U. Scheuermann, “*Measuring Thermal Resistance of Power Modules* “; PCIM Europe, May, 2003

Transient Thermal Impedance

When switching on a “cold” module, the thermal resistance R_{th} appears smaller than the static value as given in the data sheets. This phenomenon occurs due to the internal thermal capacities of the package. These thermal capacities are “uncharged” and will be charged with the heating energy resulting from the losses during operation. In the course of this charging process the R_{th} value seems to increase. During this time it is therefore called transient thermal impedance Z_{th}. When all thermal capacities are charged and the heating energy has to be emitted to the ambience, the transient thermal resistance Z_{th} has reached static data sheet value R_{th}.

The advantage of this behaviour is the short-term overload capability of the power module.

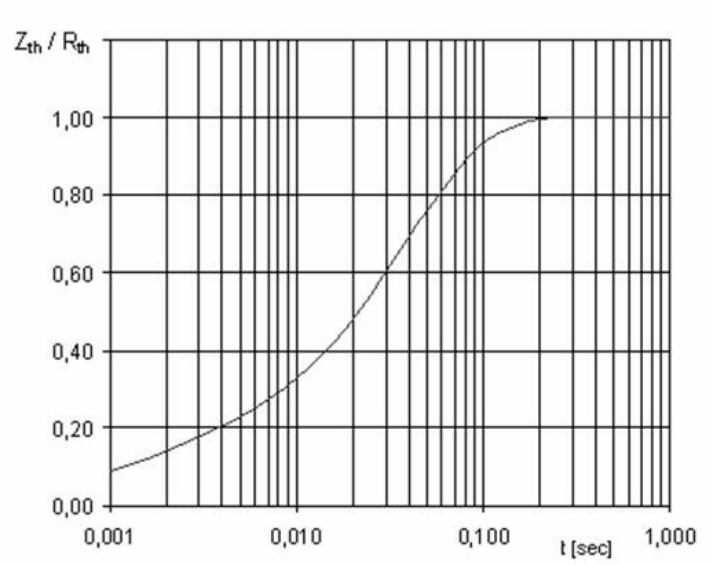


Fig.5 Example for the transient Thermal Impedance junction to case

During SEMIKRON's module qualification process the transient thermal behaviour is measured. On the basis of this measurement mathematical model is derived, resulting in the following equation (2):

$$Z_{th}(t) = R_1\left(1 - e^{\frac{t}{\tau_1}}\right) + R_2\left(1 - e^{\frac{t}{\tau_2}}\right) + ... + R_n\left(1 - e^{\frac{t}{\tau_n}}\right) \qquad (2)$$

For SEMIPACK modules, the coefficients R_n, τ_n, please refer to the tables on page 16 "Transient thermal impedance analytical elements" in data book).

Surge overload current

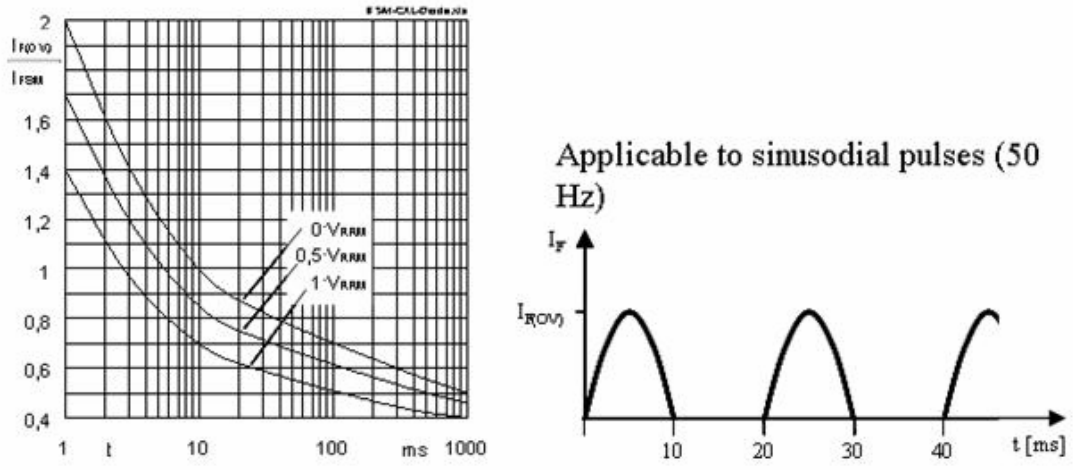


Fig.6 Surge overload current vs. time

Peak value of overload current $I_{T(OV)}$ permissible under fault conditions normalised to the surge on-state current I_{TSM} shown as a function of the duration of the fault t. The parameter is the peak reverse voltage to be reapplied immediately after the fault current has ceased. For faults lasting longer then 10 ms the graph assumes the current waveform to be a series of half sinewaves of 8.3 or 10 ms duration occurring at a rate of one every 16.6 or 20 ms.

0· V_{RRM}: no reverse voltage reapplied,

½· V_{RRM}: a voltage equal to half the repetitive peak reverse voltage rating reapplied,

1· V_{RRM}: a voltage equal to the full repetitive peak reverse voltage rating reapplied.

Insulation test

The insulation voltage of SEMIPACK modules is a guaranteed value for the insulation between the terminals and the base plate. The limiting value 3.6 KVrms specified for 1 s is subject to 100% production testing.

All terminals – including the gate connections - must be interconnected during dielectric testing. All specifications for the final products dielectric test voltage are described in the IEC publications IEC 60146-1-1.

Tests using change of temperature

Since the external contacts have a significantly higher thermal expansion coefficient than the silicon chip, it is apprant that temperature cycling, which stresses these external contacts, is in turn a particularly good test for checking the load cycling stability of the internal contacts. The test can be carried out by using the same methods as described in the above section for the testing for leaks in the encapsulation using thermal cycling. After the testing, the first criteria used for checking whether the contacts have withstood the stresses imposed, is to check the thermal resistance, but additionally the forward and reverse characteristics are checked.

Thermal cycling load tests using pulsed loading and constant cooling

Tests which use external heating and cooling of the component deviate from actual operation conditions in so far as here the component under test is uniformally heated and cooled, whereas in reality a varying temperature grandient occurs between the silicon chip and the outside. Therefore it is recommended, particularly for the type

tests of a newly development component, that a further test method is used, which makes it possible in a short time to go through a large number of cycles giving similar stresses to those which occur in the actual working environment. To achieve this the component under test is brought in close contact with a water cooled heatsink, so that the case temperature is kept almost constant, and by applying short, high current pulses the silicon chip is cyclically heated up to almost its maximum allowable virtual junction temperature. During the intervals between the pulses the junction cools down very rapidly. This method produces periodically a high temperature gradient between the silicon chip and the mounting surface.

Standard Tests for Qualification

The objectives of the test programme are:

1. To ensure general product quality and reliability.

2. To evaluate design limits by performing stress tests under a variety of test conditions.

3. To ensure the consistency and predictability of the production processes.

4. To appraise process and design changes with regard to their impact on reliability.

Following table lists the standard tests for qualifications:

	Standard Test Conditions for	
Reliability Test	**MOS / IGBT Products:**	**Diode / Thyristor Products:**
High Temperature Reverse Bias (HTRB) *IEC 60747*	1000 h, 95% V_{DSmax}/V_{CEmax}, $125°C \leq T_c \leq 145°C$	1000 h, DC, 66% of voltage class, $105°C \leq T_c \leq 120°C$
High Temperature Gate Bias (HTGB) *IEC 60747*	1000 h, $\pm V_{GSmax}/V_{GEmax}$, T_{vjmax}	not applicable
High Humidity High Temperature Reverse Bias (THB) *IEC 60068-2-67*	1000 h, 85°C, 85% RH, V_{DS}/V_{CE} = 80% V_{DSmax}/V_{CEmax}, max. 80V, V_{GE} = 0V	1000 h, 85°C, 85% RH, V_D/V_R = 80% V_{Dmax}/V_{Rmax}, max. 80V
High Temperature Storage (HTS) *IEC 60068-2-2*	1000 h, T_{stgmax}	1000 h, T_{stgmax}
Low Temperature Storage (LTS) *IEC 60068-2-1*	1000 h, T_{stgmin}	1000 h, T_{stgmin}
Thermal Cycling (TC) *IEC 60068-2-14 Test Na*	100 cycles, T_{stgmax} - T_{stgmin}	25 cycles, 100 cycles (capsule) T_{stgmax} - T_{stgmin}
Power Cycling (PC) *IEC 60749-34*	20.000 load cycles, ΔT_j = 100K	10.000 load cycles, 20.000 load cycles (capsule) ΔT_j = 100K
Vibration *IEC 60068-2-6 Test Fc*	Sinusoidal sweep, 5g, 2 h per axis (x, y, z)	Sinusoidal sweep, 5g, 2 h per axis (x, y, z)
Mechanical Shock *IEC 60068-2-27 Test Ea*	Half sine puls, 30g, 3 times each direction (±x, ±y, ±z)	Half sine puls, 30g, 3 times each direction (±x, ±y, ±z)

Fig.7 SEMIKRON standard test for product qualification

More detail to the above specified quality test or specific test results are available upon request. A complete essay is available for customer presentatation. Please contact SEMIKRON SEMIPACK® Product Management.

Lifetime Calculations

The lifetime of a power module is limited by mechanical fatigue of the package. This fatigue is caused by thermally induced mechanical stress caused by different coefficients of thermal expansion (CTE). This means that in the course of heating (power on) and cooling (power off) = temperature swing (power cycle), the materials try to expand differently on account of their different CTEs. Since the materials are joined, however, they are unable to expand freely, leading to the aforementioned thermally induced mechanical stress.

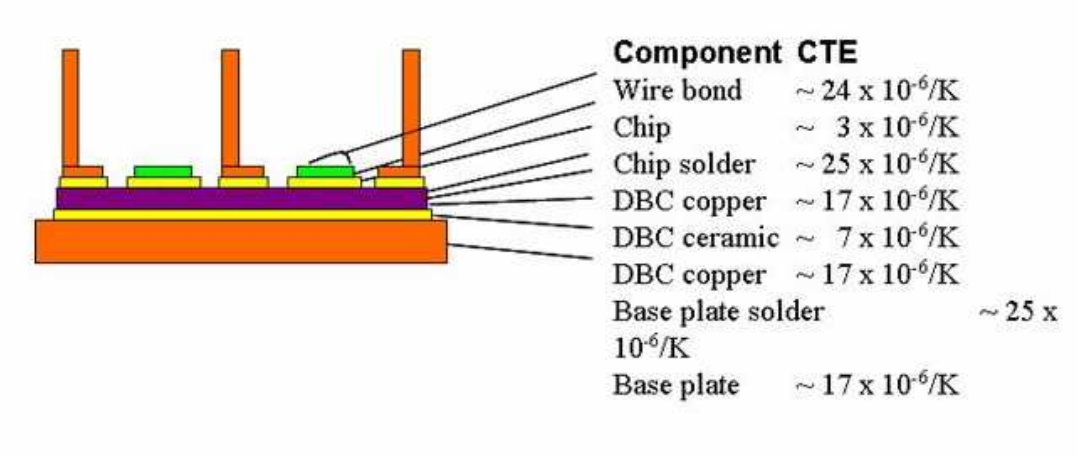


Fig.8 Cross sectional vies of SEMIPACK package, including the coefficients of thermal expansion (at 20 ℃)

When temperature changes, the mechanical stresses, that occur inside the different material layers, lead to material fatigue. The bigger the temperature difference (ΔT), the more stress is induced. With every temperature cycle aging takes place. Wire bonding and solder layers are particularly affected by this. In time aging results in small cracks which start at the edges and increase in the direction of the centre of the material with every power cycle that occurs. The higher the medium temperature $T_j m$, the faster the cracks grow, because the activating energy is higher.

The typical resulting failure picture from field returns is “lift off” of the wire bonds. This means that the cracks meet in the centre and open the connection such that the wire bond is loose.

This shows that the lifetime is determined by the number of temperature cycles which can be withstood by the module. In the 90’s intensive investigations were carried in this area, including a research project known as the “LESIT study”. One of the main findings of this study was the equation given below (7-1), which shows relationship

between the number of cycles Nf and the junction temperature difference ΔT_j and the medium temperature $T_j m$.

SEMIPACK modules are based on the same design principles as the modules which were investigated in the course of the LESIT study. For this reason the LESIT results may be used for life time estimations. That said, the reliability of power modules has improved since the LESIT study was concluded, which is why the results of equation (7-1) can be seen as a worst-case scenario.

$$Nf = A \times \Delta T_j^{\alpha} \times \exp\left(\frac{Q}{R \times T_j m}\right) \qquad (3)$$

With A = 640, α = -5, Q = 7.8 10^{-4} J/mol and R = 8.314 J/mol K; ΔT_j and $T_j m$ in [K]

Fig.9 shows the experimental results of the LESIT study (as bullet points) as well as the results of equation (3) as drawn lines.

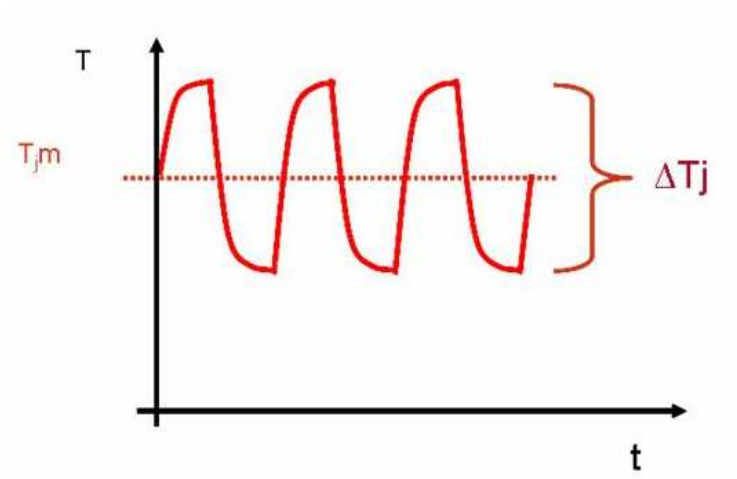


Fig.9 Example of $T_j m$ and ΔT_j

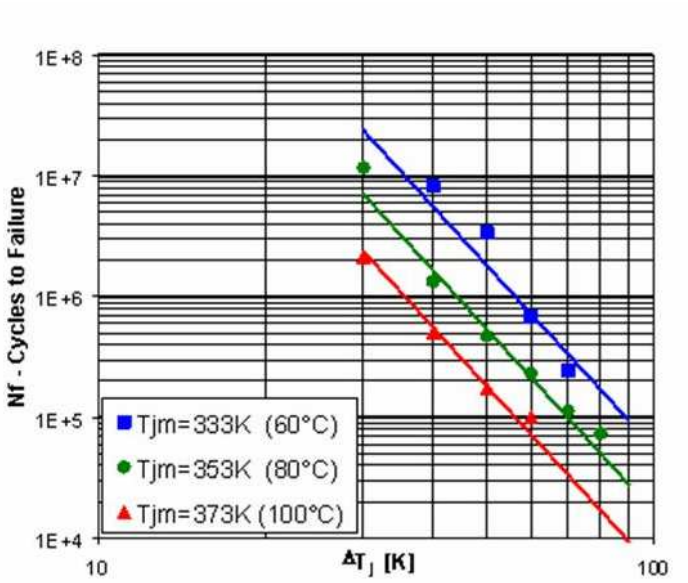


Fig.10 "LESIT" curves, based on experimental results

For further information on the lifetime calculations for power modules please refer to:

M. Held et.al., "*Fast Power Cycling Tests for IGBT Modules in Traction Application*"; Proceedings PEDS, pp 425 – 430, 1997

Application

The terms in [ ] apply solely to thyristors

Voltage class selection

The table below contains the recommended voltage class allocations for the repetitive peak reverse voltages V_{RRM} [V_{DRM}] of SEMIPACK® modules and rated AC input voltage V_{VN}.

Rated AC voltage L-L	Recommended peakreverse voltage
VDRM	V_{RRM}, [V_{DRM}] / V
60	200
125	400
250	800
380	1200
400	1400
440	1400
460	1600
500	1600
575	1800
660	2200
690	2200

Fig.1 recommended voltage class allocations for the repetitive pear reverse toltages V_{RRM}[V_{DRM}]

As detailed in the technical explanations, the maximum permissible value for direct reverse voltages (continuous duty) across diode (V_R) [or thyristors (V_D, V_R)] in statinary operations is 0.7 V_{RRM} [0.7 V_{DRM}].

Overvoltage protection

It is well known that single crystal semiconductor devices are sensitive to over-voltages. Every time their specified reverse voltage is exceedet it can lead to their destruction. It is therefore necessary to protect silicon diodes and thyristors against voltage transients however caused, i.e. the transient voltages must be reduced to values below the maximum specified limits for the semiconductor device.

A variety of well tried and tested coponents are suitable for the above suppression. The most important are:

- Resistors and capacitors (RC snubber networks)

- varistors
- silicon avalanche diodes

The RC networ perates by forming with existing inductances a series resonant circuit wihich transforms any steeply rising transient voltage into a damped sinewave of lower amplitude. Thk power of the voltage transient is converted from a high value of short duration to a lower value extending over a longer period of time.

All the other components listed above make use of non-linear characteristics. Their internal resistances reduce as the applied voltage increases such that, together with the other risistances and inductances in the circuit, they build non-linear voltage dividers which allow througu low voltages unattenuated but clip high voltages above a difined level. The energy of the transient voltage is again spread over a longer period, and is almost completely absorbed by the suppression component.

The suppression components can be positioned on the a.c. side of the diode or thyristor stack, on the d.c. side, or across each semiconductor device in the circuit. The advantages and disadvantages of these various arrangements will be considered separately for each type of suppression component.

RC snubber circuit are often connected in parallel to the diode [thyristor] to provide protection from transient overvoltage, although in some cases varistors are used. Due to the RC circuit the rate of rise of voltage is limited during commutation, which reduces the peak voltages across the circuit inductors.

Over-current and short circuit protection

If short circuit protection is required for the diodes, [thyristors], (urtra fast) semiconductor fuses are used. These are to be dimendioned on the basis of the forward current and i^2t value.

Other types of protection for high current circuits are, for example, fuses which isolate damaged diodes [thristors] from the parallel connections. To protect components from statically non-permissible high overcurrents, it is possible to use magnetic or thermal overcurrent circuit breakers of temperature semsors on the heat sinks. Although these do not detect dynamic overload within a circuit. For this reason, temperature sensors are used mainly with forced air cooling in order to protect damage to the diodes [thyristors] in the event of fan failure.

Over-current and short

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Permissible over currents

The permissible forward currents for short-time or intermediate operation, as wess as for frequencies below 40 Hz are to be calculated on the basis of the transient ghermal impedance or the thermal impedance under pulse conditions so that the virtual junction temperature Tvj does not exceed the maximum permissible value at any time.

FAQ for applications

1. Difference between SKKT.../ and SKKT...B

Description: What is the difference between SEMIPACK Thyristor modules with and without the extension B (for example SKKT57 and SKKT57B)?

Solution: The difference is the arrangement of the control connectors Gate (G) and Auxiliary Cathode (K), concerning SEMIPACK1 with 4 auxiliary connectors only.

For SKKT20/ to SKKT106/: G1/K1 G2/K2

For SKKT20B to SKKT106B : G1/K1 K2/G2

Aim is to have a second source for competitor products.

2. Derating of rectifier current at higher frequencies

Description: Is a derating of the rectifier current necessary at higher frequencies?

Solution: Line rectifiers like diodes or thyristors are usable without current derating in a frequency range of 16.66Hz to 400Hz. Above this frequency you need a derating, because of the normally neglected switching losses.

3. MTBF value: Failure rate is the frequency with which an engineered system or component fails, expressed for example in failures per hour. It is often denoted by the Greek letter λ (lambda) and is important in reliability theory.

$\Lambda = FIT = \frac{n_f}{N \cdot t}$

n_f= Number of observed failures

N= Number of obserec componets

T= Observation time

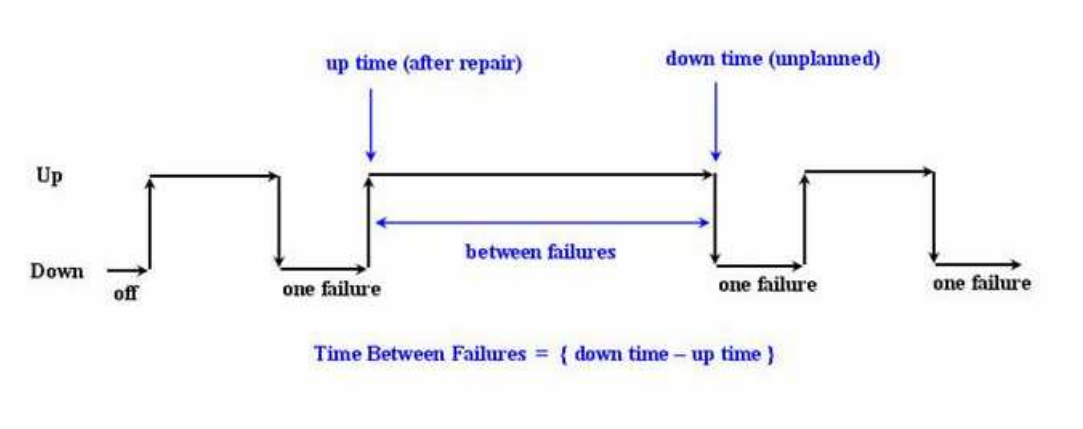

Fig.2 Information about the calculation of reliability

In practice, the reciprocal rate MTBF is more commonly expressed and used for high quality components or systems.

Mean time between failures (MTBF) is the mean (average) time between failures of a system, and is often attributed to the “useful life” of the device i.e. not including ‘infant mortality’ or ‘end of life’ if the device is not repairable. Calculations of MTBF assume that a system is “renewed” i.e. fixed, after each failure, and then returned to service immediately after failure. The average time between failing and being returned to service is termed mean down time (MDT) or mean time to repair (MTTR).

More information: *http://de.wikipedia.org/wiki/Mean_Time_Between_Failures*

MTBF values given below are appraised according to customer returns and we haven't done any measurements about it. Therefore, the values are only for reference. We can not guarantee them.

Product	Fit	MTBF (x 10^8h)
Semipack 1	70	0,14
Semipack 2	50	0,2
Semipack 3	50	0,2
Semipack 4	50	0,2
Semipack 5	50	0,2

Fig.3 FIT and MTBF values of SEMIPACK products

4. Why SEMIKRON defines the min. V_{GT} and I_{GT}, however, some competitors give max.V_{GT} and I_{GT} values in their data sheet?

Due to the following reason SEMIKRON are I_{GT} and V_{GT} in data sheet as min. values specified:

In the chapter "Modules-Explanations-SEMIPACK" in our data sheet catalogue the definition of I_{GT} and V_{GT} is: Minimum values for square-wave triggering pulses lasting longer than 100us or for d.c. The values are necessary to fire a thyristor at Tvj=25℃ properly. Therefore, we give the min. I_{GT} and V_{GT} values in our data sheet.

The max. I_{GT} and V_{GT} values given in Infineon data sheet are sometimes called highest gate current/voltage, which can not be exceeded in order to keep thyristor being not fired. i.e. customer can apply max. IGT and VGT values on thyristor without firing the thyristor.

Both definitions have same meaning and are only expressed in different way.

5. Resistance of semiconductor:

It's impossible to measure the resistance of a semiconductor with a Ohm meter.

Reasons are the leakage current and the nonlinear characteristics of semiconductor, which can vary over several decades

The gate - cathode terminals can be checked with a "diode" function of a multimeter, but not with the resistor function.

Accessories

For SEMIPACK 1,2,3,4 there are complete kits available:

Hardware needed for one SEMIPACK®	SEMIPACK® 1 a) SKKD/E 26...100 b) SKKT/H/L 20...106	SEMIPACK® 2 SKKT/H 122...162 SKKD/E 162, SKKD 212	SEMIPACK® 3 SKKT/H/L 213...330 SKKD/E 260,380	SEMIPACK® 4 SKET 330, 400 SKKE 400
Gate female plug Insulating sleeve Double olug caps Baseplate screws Terminal screws Washers Spring washers	b: 2 pcs.2,8×0,8 mm[3] b: 4 pcs. 2 pcs. M5×18 socket head 3 pcs. M5×10 pozidrive head captive captive	4 pcs. 2,8×0,8mm[4] - 2 pcs. (right+left) 2 pcs. M5×18 socket head 3 pcs. M6×12 pozidrive head (3 pcs. 6,4 mm Φ) (3 pcs. 6,4 mm Φ)	4 pcs.2,8×0,8mm[4] - 2 pcs. (right+left) 4 pcs. M5×18[2] socket head 3 pcs. M8×16, hexagon head capative capative	2 pcs. 2,8×0,8 mm[4] - 1 pcs. (right) 4 pcs. M5×18[2] socket head 2 pcs. M10×50[1] 2 pcs. 10,5 mm Φ
Part No. of the complite kit	for 12 SEMIPACKs a: 33704200 b: 33403900	for 8 SEMIPACKs 33404000	for 3 SEMIPACKs 33404100	for 3 SEMIPACKs 33404500

Fig.1 Mounting hard ward for SEMIPACK modules

[1] Spindle No. 30143660 with 2 nuts M 10

[2] For SEMIPACK 3 with 10 mm thick base plates and SEMIPACK 4 on heat sink P3, use M5×20(No. 30145490), available on request

All accessories can also be ordered separately,

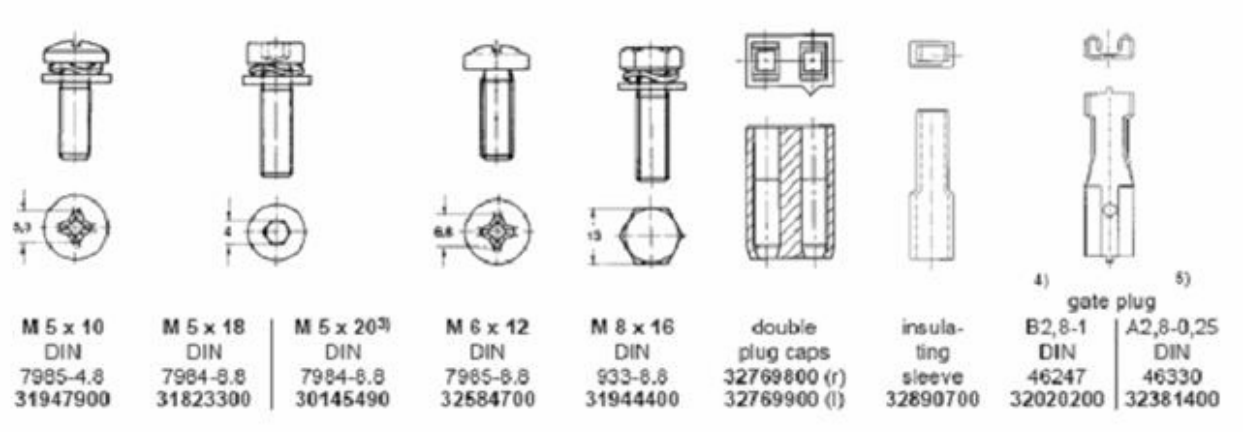

Fig.2 Mounting screws for SEMIPACK Modules

Two different double plug caps are available, 32769800(r) has a right nose and 32769900(l) has a left nose. 32769800(r) is used for terminals 4 and 5 of SEMIPACK

2,3,4,5; 32769900(l) is used for terminals 6 and 7 of SEMPACK 2,3,5 and SEMIPACK 6.

Logistics

Laser Marking on modules

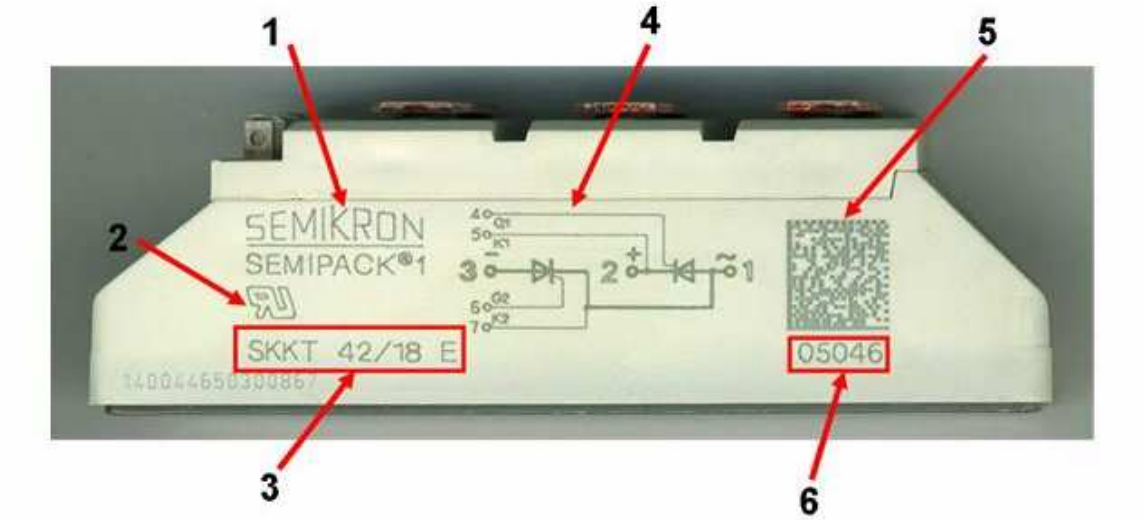

Fig.1 Typical laser marking of SEMIPACK module

1	SEMIKRON logo, with product line designation “SEMIPACK®”
2	UL logo, SEMIPACK is UL recognised, file name: E63532
3	Type designation
4	Circuit diagram
5	Data Matrix Code
6	Date code – 5 digits: YYMML (L = Lot of same type per week)

Data Matrix Code

The Data Matrix Code contains following information:

- *Type description*
- *Part number*
- *Measurement line number*
- *Production tracking number*
- *Data code*
- *Continuous number*

Packing box

Fig.2 Standard Packing boxes for SEMIPACK modules

Quantities per package:

SEMIPACK 0: 21 pieces

SEMIPACK 1: 12 pieces

SEMIPACK 2: 8 pieces

SEMIPACK 3: 3 pieces

SEMIPACK 4: 3 pieces

SEMIPACK 5: 2 pieces

SEMIPACK 6: 1 piece

Marking packing boxes

Fig.3 Lable of SEMIPACK packing boxes

1. SEMIKRON logo
2. Type designation
3. Data code
4. SEMIKRON part number – also as bar code
5. Quantity - also as bar code